Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (canceled).

Claim 2 (currently amended): The apparatus according to claim ~~1~~6, wherein said logic circuit further comprises a NAND gate.

Claim 3 (original): The apparatus according to claim 2, wherein said NAND gate further comprises:

a plurality of transistors connected in parallel having a plurality of inputs and at least one output.

Claim 4 (currently amended): The apparatus according to claim ~~1~~6, further comprising an enable logic gate connected to said at least one output of said logic circuit.

Claim 5 (currently amended): The apparatus according to claim ~~1~~6, further comprising a transistor configured as an open collector having an input and an output whose input is connected to said at least one output of said logic circuit.

Claim 6 (currently amended): An apparatus for safe insertion and removal of a circuit board for hot swap applications comprising ~~The apparatus according to claim 1~~:

a logic circuit having at least one input and at least one output; and

a time extender circuit connected to said logic circuit, for extending an output signal of said logic circuit for a period of time after said circuit board is completely inserted and removed, wherein said time extender circuit further comprises:

a resistor connected between ground and said logic circuit; and

a capacitor connected between a voltage and said logic circuit.

Claim 7 (original): The apparatus according to claim 2, further comprising at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate.

Claim 8 (original): The apparatus according to claim 3, further comprising at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to said at least one output of said plurality of transistors.

Claim 9 (original): The apparatus according to claim 7, wherein said at least one inverter is a Schmitt trigger inverter.

Claim 10 (original): The apparatus according to claim 8, wherein said at least one inverter is a Schmitt trigger inverter.

Claim 11 (original): The apparatus according to claim 8, further comprising:

an enable logic gate connected to at least one of said outputs of said at least one inverter; and

a transistor configured as an open collector having an input and an output whose input is connected to at least one of said outputs of said at least one inverter.

Claim 12 (currently amended): An apparatus for indicating the insertion and removal of a circuit board, comprising:

a plurality of transistors connected in parallel having at least two inputs and at least one output;

at least one other transistor having at least one output and at least one input connected to said at least one output of said plurality of transistors connected in parallel;

at least one Schmitt trigger inverter having an input connected to said output of said at least one other transistor; and

a time extender circuit connected to said at least one output of said at least one other transistor, wherein said time extender circuit further comprises:

a resistor connected between ground and said logic circuit; and

a capacitor connected between a voltage and said logic circuit.

Claim 13 (original): The apparatus according to claim 12, further comprising a transistor configured as an open collector having an input and an output whose input is connected to said output of said at least one Schmitt trigger inverter.

Claims 14-23 (canceled).

Claim 24 (new): The apparatus according to claim 12, further comprising:

an enable logic gate connected to at least one of said outputs of said at least one Schmitt trigger inverter.

Claim 25 (new): The apparatus according to claim 24, further comprising:

a transistor configured as an open collector having an input and an output whose input is connected to at least one of said outputs of said at least one Schmitt trigger inverter.